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| state.vhd  library ieee;  use ieee.std\_logic\_1164.all;  use ieee.std\_logic\_arith.all;  use ieee.std\_logic\_unsigned.all;  entity state is  port(  start:in std\_logic;  in1:in std\_logic\_vector(3 downto 0);  in2:in std\_logic\_vector(3 downto 0);  sonuc:out std\_logic\_vector(3 downto 0);  clk,reset:in std\_logic  );  end state;  architecture beh of state is  type typ\_state is (A,B,C);  signal state,next\_state:typ\_state;  signal ara\_in1,ara\_in2,ara\_sonuc:std\_logic\_vector(3 downto 0):="0000";  begin  process(clk,reset)  begin  if(reset='1')then  state<=A;  elsif(rising\_edge(clk))then  state<=next\_state;  end if;  end process;  process(state,start,ara\_in2)  begin  case state is  when A=>  if(start='1') then  next\_state<=B;  else  next\_state<=A;  end if;  when B=>  if(ara\_in2="0001") then  next\_state<=C;  else  next\_state<=B;  end if;  when C=>  next\_state<=C;  end case;  end process;  process(clk)  begin  case state is  when A=>  ara\_in1<=in1;  ara\_in2<=in2;  ara\_sonuc<="0000";  when B=>  ara\_sonuc<=ara\_sonuc+ara\_in1;  ara\_in2<=ara\_in2-"0001";  when C=>  sonuc<=ara\_sonuc;  end case;  end process;  end beh; |